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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,214	08/08/2001	Ted Moise	10003787-1	3138

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EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
	2826

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Applicant No. 09/925,214	Applicant(s) MOISE ET AL.
	Examiner Thomas L Dickey	Art Unit 2826

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

THE REPLY FILED 14 November 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) The period for reply expires _____ months from the mailing date of the final rejection.
- b) The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. The proposed amendment(s) will not be entered because:
 - (a) they raise new issues that would require further consideration and/or search (see NOTE below);
 - (b) they raise the issue of new matter (see Note below);
 - (c) they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 - (d) they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. Applicant's reply has overcome the following rejection(s): _____.
4. Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. The a) affidavit, b) exhibit, or c) request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
6. The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. For purposes of Appeal, the proposed amendment(s) a) will not be entered or b) will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: 41 and 59.

Claim(s) rejected: 39,40,57,58 and 71-74.

Claim(s) withdrawn from consideration: _____

8. The drawing correction filed on _____ is a) approved or b) disapproved by the Examiner.

9. Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.

10. Other: _____

Minhloan Tran
Minhloan Tran
Primary Examiner
Art Unit 2826

Continuation of 5. does NOT place the application in condition for allowance because:

As a preliminary matter it is noted that claims 39,57,71, and 73 currently read:

39. (amended) An integrated circuit comprising: a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having at least one contact via extending there through; a ferroelectric device level, positioned over the transistor isolation layer, the ferroelectric device level including at least one ferroelectric capacitor, and an overlying ferroelectric isolation layer having at least one via extending there through and aligned with a corresponding contact via, the via extending through the ferroelectric isolation layer being laterally sized larger than the corresponding contact via aligned therewith, a first metal level, an inter-level dielectric level disposed over the first metal layer; a second metal level disposed over the inter-level dielectric level.

71. (new) An integrated circuit, as defined in claim 39, wherein between the ferroelectric device level and the transistor isolation layer is free of any interposing metal level.

57. (amended) A method of forming an integrated circuit, comprising: forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having at least one contact via extending therethrough; forming a ferroelectric device level over the transistor isolation layer, the ferroelectric device level including at least one ferroelectric capacitor, and an overlying ferroelectric isolation layer having at least one via extending there through and aligned with a corresponding contact via, the via extending through the ferroelectric isolation layer being laterally sized larger than the corresponding contact via aligned therewith, forming a first metal level, forming an inter-level dielectric level over the first metal layer; forming a second metal level disposed over the inter-level dielectric level.

73. (new) A method of forming an integrated circuit, as defined in claim 57, wherein between the ferroelectric device level and the transistor isolation layer is free of any interposing metal level.

It is argued, under section IIA of the remarks, that "No one of ordinary skill in the art at the time of the invention could have considered the dielectric layer 14 to be a 'ferroelectric device level including at least one ferroelectric capacitor,' as asserted by the Examiner."

Applicant and Examiner agree that the cited art discloses a device level 14 including part of at least one ferroelectric capacitor. Applicant argues that the claim language "including at least one ferroelectric capacitor," means "containing at least one ferroelectric capacitor in its entirety," to the *cognoscenti*. However, whether the *cognoscenti* so construe it, or not, is immaterial. Claims are to be construed, firstly according to their plain meaning, secondly according to a meaning imparted by the specification in such a way that it is clear from the specification that applicant means to give up any broad coverage imparted from a plain reading, and finally, but only in the event of an ambiguity in the plain meaning, according to

extrinsic evidence such as what one of ordinary skill in the art at the time of the invention could have considered the claim to mean. See *Bell & Howell Document Management Products Co. v. Altek Systems* 45 USPQ2d 1033, 1038 (CA FC, 1997). The plain meaning of “including at least one ferroelectric capacitor,” is not ambiguous.

It is further argued, under section IIA of the remarks, that “[layer 16 is not an ‘overlying ferroelectric isolation layer’ because] layer 16 does not lie over either of the two capacitors... [and because] layer 16 does not function as a ‘ferroelectric isolation layer’ for the ferroelectric capacitors.” However, here applicant argues limitations not found in either claim 39 or claim 57. These two claims simply require that the “ferroelectric isolation layer” be “overlying,” without specifying what is overlain, and that the “ferroelectric isolation layer” isolate something, without specifying what is isolated.

It is argued, under section IIB of the remarks, that “both [wiring layer 9 and wiring layer 11] are interposed between the dielectric layer 14 and the dielectric layer 8.” Applicant’s argument is premised on the supposition that Kimura et al. discloses only metallic wiring layers and thus layers 9 and 11 cause the disclosed device to fail to meet the limitation “free of any interposing metal level.” However, at paragraph 34 Kimura et al. discloses that layers 9 and 11 may be formed of tungsten, copper (both admittedly metals) or silicide. Silicide is not a metal.